

Thyristor Surge Suppressors (TSS)

P0080TA - P5000TA Series - DO-214AC(SMA)

@10/700 μ S , 2KV

Description

P0080TA - P5000TA Series are designed to protect broadband equipment such as modems, line card, CPE and DSL from damaging over-voltage transients.

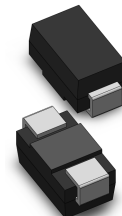
The series provides a surface mount solution that enables equipment to comply with global regulatory standards.

Features and Benefits

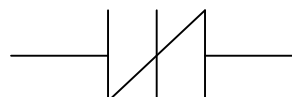
- u Low voltage overshoot
- u Low on-state voltage
- u Does not degrade surge capability after multiple surge events within limit
- u Fails short circuit when surged in excess of ratings
- u Low Capacitance

Applicable Global Standards

- u TIA-968-A
- u ITU K.20/21 Enhanced level
- u ITU K.20/21 Basic Level
- u GR 1089 Inter building
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- u IEC 6100-4-5
- u YD/T 1082
- u YD/T 993
- u YD/T 950

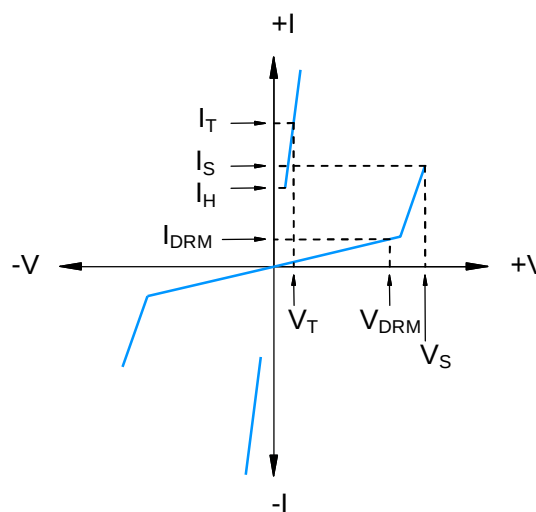


Schematic Symbol



Electrical Parameters

Parameter	Definition
I_S	Switching Current - maximum current required to switch to on state
I_{DRM}	Leakage Current - maximum peak off-state current measured at V_{DRM}
I_H	Holding Current - minimum current required to maintain on state
I_T	On-state Current - maximum rated continuous on-state current
V_S	Switching Voltage - maximum voltage prior to switching to on state
V_{DRM}	Peak Off-state Voltage - maximum voltage that can be applied while maintaining off state
V_T	On-state Voltage - maximum voltage measured at rated on-state current
C_0	Off-state Capacitance - typical capacitance measured in off state



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Part Number	Marking	V_{DRM} @ $I_{DRM}=5\mu A$	I_{DRM}	V_S @ $100V/\mu S$	I_S	V_T @ $I_T=2.2A$	I_T	I_H	C_o @ $1MHz$
		V min	μA max	V max	mA max	V max	A max	mA min	pF max
P0080TA	P008A	6	5	25	800	4	2.2	50	50
P0300TA	P03A	25	5	40	800	4	2.2	50	70
P0640TA	P06A	58	5	77	800	4	2.2	150	50
P0720TA	P07A	65	5	88	800	4	2.2	150	50
P0900TA	P09A	75	5	98	800	4	2.2	150	45
P1100TA	P11A	90	5	130	800	4	2.2	150	45
P1300TA	P13A	120	5	160	800	4	2.2	150	45
P1500TA	P15A	140	5	180	800	4	2.2	150	40
P1800TA	P18A	170	5	220	800	4	2.2	150	40
P2000TA	P20A	180	5	220	800	4	2.2	150	40
P2300TA	P23A	190	5	260	800	4	2.2	150	35
P2600TA	P26A	220	5	300	800	4	2.2	150	35
P3100TA	P31A	275	5	350	800	4	2.2	150	30
P3500TA	P35A	320	5	400	800	4	2.2	150	30
P3800TA	P38A	360	5	460	800	4	2.2	150	30
P4200TA	P42A	400	5	520	800	4	2.2	150	30
P4500TA	P45A	420	5	540	800	4	2.2	150	30
P5000TA	P50A	440	5	600	800	4	2.2	150	30

Notes:

- Absolute maximum ratings measured at $T_A=25^{\circ}C$ (unless otherwise noted).
- Devices are bi-directional.

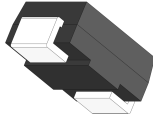
Surge Ratings

Series	$2/10\mu S^1$	$8/20\mu S^1$	$10/160\mu S^1$	$10/560\mu S^1$	$10/1000\mu S^1$	$5/310\mu S^1$	I_{TSM} 50/60 Hz	di/dt
	$2/10\mu S^2$	$1.2/50\mu S^2$	$10/160\mu S^2$	$10/560\mu S^2$	$10/1000\mu S^2$	$10/700\mu S^2$		
	A min	A min	A min	A min	A min	A min	A min	Amps/ μs max
A	150	150	90	50	45	50	20	500

Notes:

- Current waveform in μs
 - Voltage waveform in μs
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product.
 - I_{PP} ratings applicable over temperature range of $-40^{\circ}C$ to $+85^{\circ}C$
 - The device must initially be in thermal equilibrium with $-40^{\circ}C < T_J < +150^{\circ}C$

Thermal Considerations

Package	Symbol	Parameter	Value	Unit
DO-214AC 	T_J	Operating Junction Temperature Range	- 40 to + 150	$^{\circ}C$
	T_S	Storage Temperature Range	- 40 to +150	$^{\circ}C$
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	90	$^{\circ}C/W$

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Characteristic Curves

Figure 1 V-I Characteristics

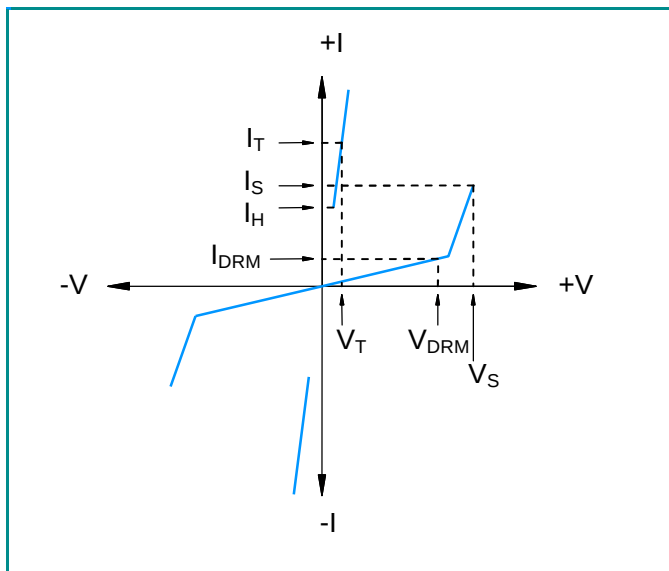


Figure 2 - $t_r \times t_d$ Pulse Waveform

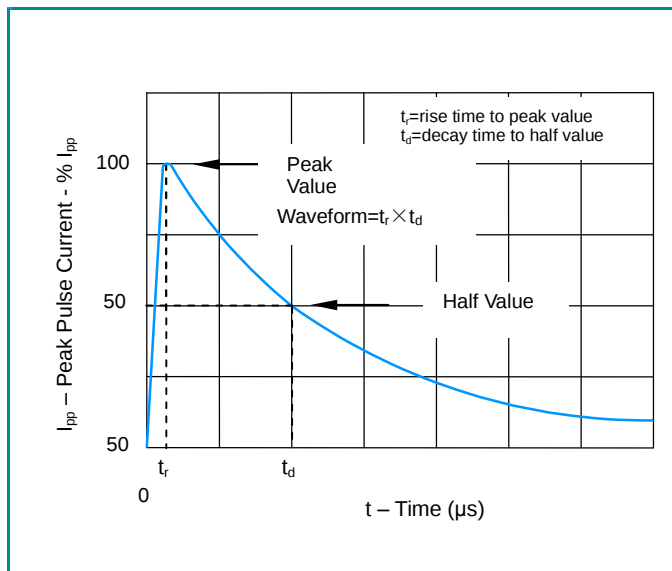


Figure 3 - Normalized V_S Change Versus Junction

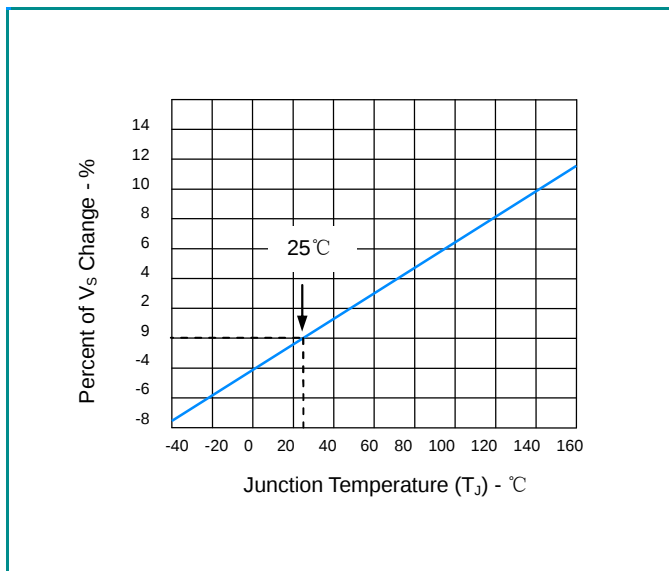
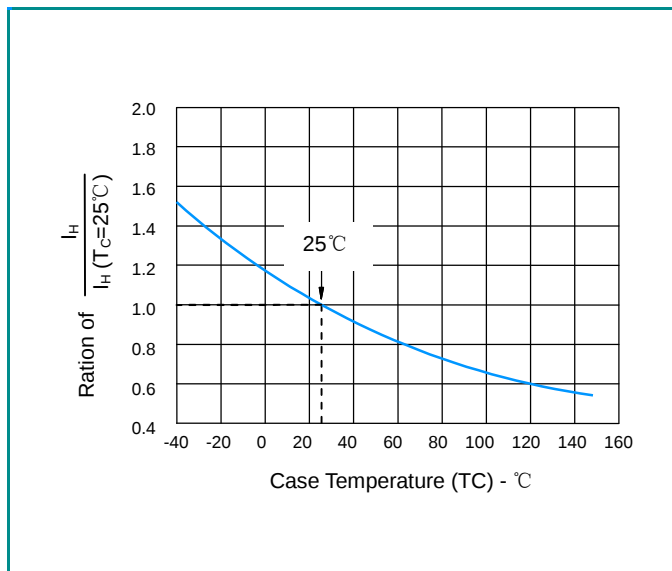


Figure 4 - Normalized DC Holding Current Versus Case



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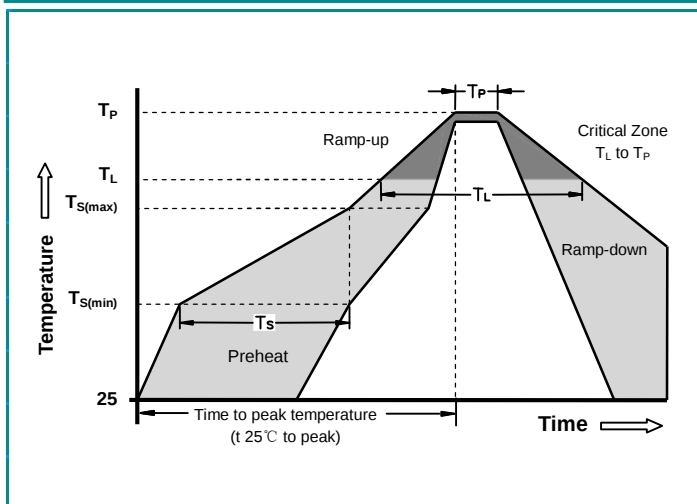
Environmental Specifications

High Temp Voltage Blocking	80% Rated VDRM (VAC Peak) +125°C or +150°C, Lead Material Copper Alloy High Temp Voltage Blocking 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65°C to +150°C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 VDC (+85°C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150°C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65°C, 1008 hrs.
Thermal Shock	0°C to +100°C, 5 min. dwell, 10 sec. transfer, Thermal Shock 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121°C, 100%RH, 2atm, 24 up to 168 hrs. EIA/Cooker Test) JEDEC, JESD22-A-102
Resistance to Solder Heat	+260°C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85°C, 168 hrs., 3 reflow cycles Level (+260°C Peak). JEDEC-J-STD-020, Level 1

Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification 94V-0

Soldering Parameters



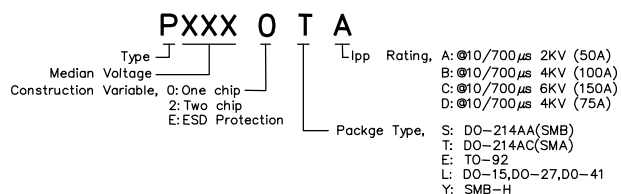
Reflow Condition		Lead-free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (min to max) (t_s)	60 -180 Seconds
Average ramp up rate (Liquidus Temp T_L) to peak		3°C/Second Max
$T_{s(max)}$ to T_L - Ramp-up Rate		3°C/Second Max
Reflow	- Temperature (T_L) (Liquidus)	+217°C
	- Time (min to max) (t_s)	60 -150 Seconds
Peak Temperature (T_P)		260 +0/-5°C
Time within 5°C of actual peak Temperature (t_p)		30 Seconds Max
Ramp-down Rate		6°C/Second Max
Time 25°C to peak Temperature (T_P)		8 minutes Max
Do not exceed		+260°C

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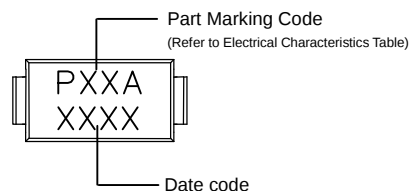
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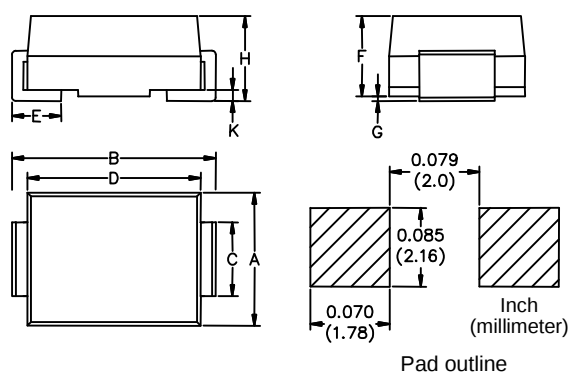
Part Numbering



Part Marking



Dimensions DO-214AC



Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.100	0.110	2.54	2.79
B	0.194	0.208	4.93	5.28
C	0.049	0.065	1.25	1.65
D	0.157	0.177	3.99	4.50
E	0.030	0.060	0.76	1.52
F	0.076	0.096	1.90	2.45
G	0.002	0.008	0.05	0.20
H	0.078	0.090	1.98	2.29
K	0.006	0.012	0.15	0.30

Packaging

Part Number	Component Package	Quantity	Packaging Option	Packaging Specification
Pxxx0TA	DO-214AC	5000	Tape & Reel -12mm/13"tape	EIA -481

Tape and Reel Specifications

