

QIAOXIN N-Channel Super Junction Power MOSFET III

General Description

The series of devices use advanced trench gate super junction technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

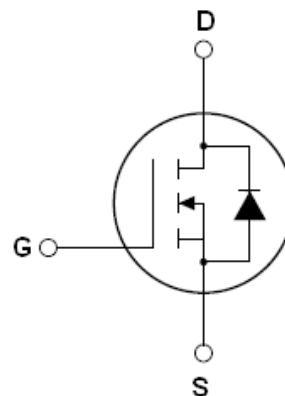
Features

- New technology for high voltage device
- Low on-resistance and low conduction losses
- Small package
- Ultra Low Gate Charge cause lower driving requirements
- 100% Avalanche Tested
- ROHS compliant

Application

- Power factor correction (PFC)
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply (UPS)

V_{DS}	650	V
$R_{DS(ON) MAX}$	199	mΩ
I_D	21	A



Schematic diagram

Package Marking And Ordering Information

Device	Device Package	Marking
VCRR65T180V	DFN8×8	VCRR65T180V

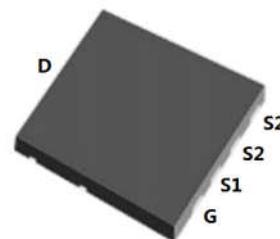


Table 1. Absolute Maximum Ratings ($T_C=25^\circ\text{C}$)

Parameter	Symbol	Value	Unit
Drain-Source Voltage ($V_{GS}=0V$)	V_{DS}	650	V
Gate-Source Voltage ($V_{DS}=0V$), AC ($f>1\text{ Hz}$)	V_{GS}	± 30	V
Continuous Drain Current at $T_C=25^\circ\text{C}$	$I_{D(DC)}$	21	A
Continuous Drain Current at $T_C=100^\circ\text{C}$	$I_{D(DC)}$	13.2	A
Pulsed drain current ^(Note 1)	$I_{DM(pluse)}$	84	A
Maximum Power Dissipation($T_C=25^\circ\text{C}$)	P_D	188	W
Derate above 25°C		1.5	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 2)	E_{AS}	441	mJ
Avalanche current ^(Note 1)	I_{AR}	10.5	A
Repetitive Avalanche energy , t_{AR} limited by T_{Jmax} ^(Note 1)	E_{AR}	0.7	mJ

DFN8×8

Parameter	Symbol	Value	Unit
Drain Source voltage slope, $V_{DS} \leq 480V$,	dv/dt	50	V/ns
Reverse diode dv/dt , $V_{DS} \leq 480V, I_{SD} < I_D$	dv/dt	15	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55...+150	°C

* limited by maximum junction temperature

Table 2. Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Maximum)	R_{thJC}	0.66	°C /W
Thermal Resistance, Junction-to-Ambient (Maximum)	R_{thJA}	62.5	°C /W

Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	650			V
Zero Gate Voltage Drain Current(Tc=25℃)	I _{DSS}	V _{DS} =650V,V _{GS} =0V		0.05	1	μA
Zero Gate Voltage Drain Current(Tc=125℃)	I _{DSS}	V _{DS} =650V,V _{GS} =0V			100	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	3	3.5	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =10.5A		170	199	mΩ
Dynamic Characteristics						
Forward Transconductance	g _{FS}	V _{DS} = 20V, I _D = 10.5A		16		S
Input Capacitance	C _{iss}	V _{DS} =50V,V _{GS} =0V, F=1.0MHz		2250		PF
Output Capacitance	C _{oss}			83		PF
Reverse Transfer Capacitance	C _{rss}			1.6		PF
Total Gate Charge	Q _g	V _{DS} =480V,I _D =21A, V _{GS} =10V		36		nC
Gate-Source Charge	Q _{gs}			14		nC
Gate-Drain Charge	Q _{gd}			8.5		nC
Switching times						
Turn-on Delay Time	t _{d(on)}	V _{DD} =380V,I _D =11A, R _G =4Ω,V _{GS} =10V		11		nS
Turn-on Rise Time	t _r			6		nS
Turn-Off Delay Time	t _{d(off)}			61		nS
Turn-Off Fall Time	t _f			4.5		nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I _{SD}	T _C =25℃			21	A
Pulsed Source-drain current(Body Diode)	I _{SDM}				84	A
Forward on voltage	V _{SD}	T _j =25℃,I _{SD} =21A,V _{GS} =0V		0.9	1.3	V
Reverse Recovery Time	t _{rr}	T _j =25℃,I _F =21A,di/dt=100A/μs		310		nS
Reverse Recovery Charge	Q _{rr}			5		uC
Peak Reverse Recovery Current	I _{rrm}			28		A

Notes 1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. $T_J=25^\circ C, V_{DD}=50V, V_G=10V, R_G=25\Omega$

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

Figure1. Safe operating area

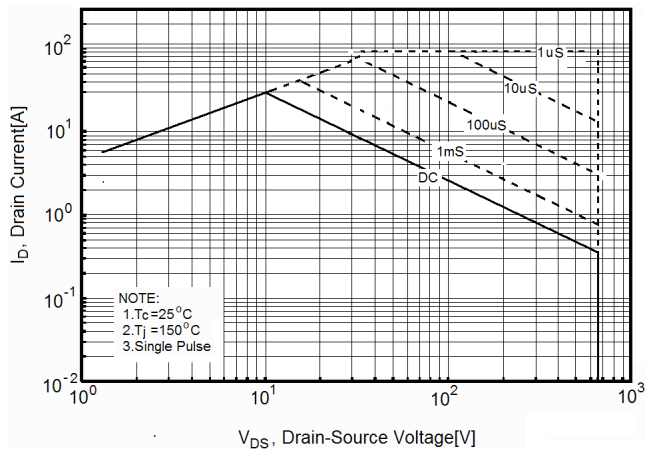


Figure2. Transient Thermal Impedance

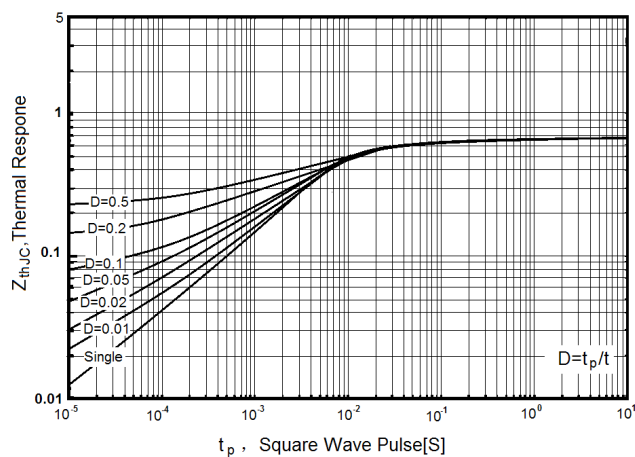


Figure3. Source-Drain Diode Forward Voltage

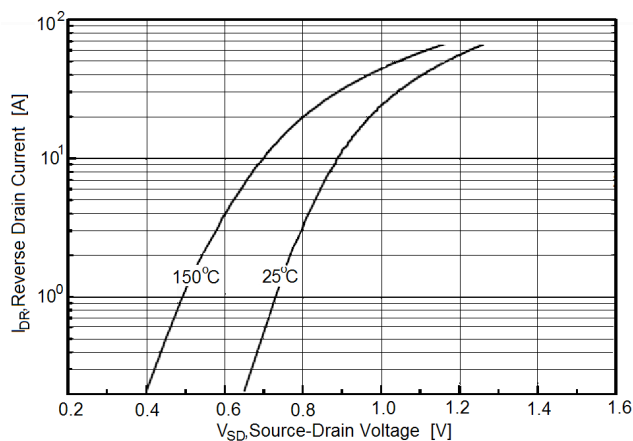


Figure4. Output characteristics

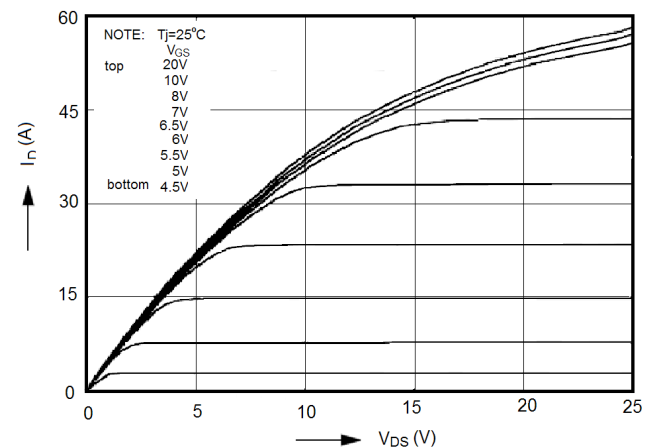


Figure5. Transfer characteristics

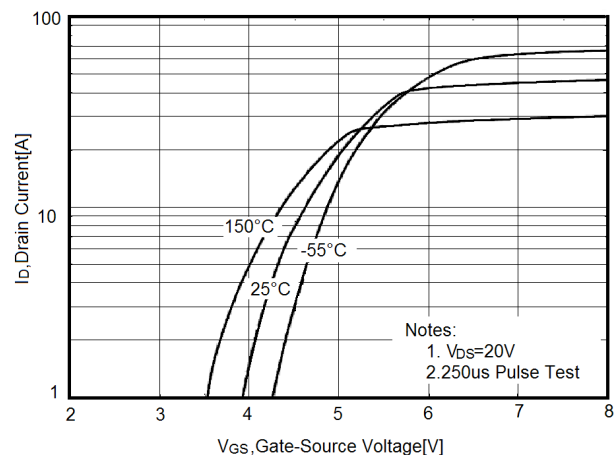


Figure6. Static drain-source on resistance

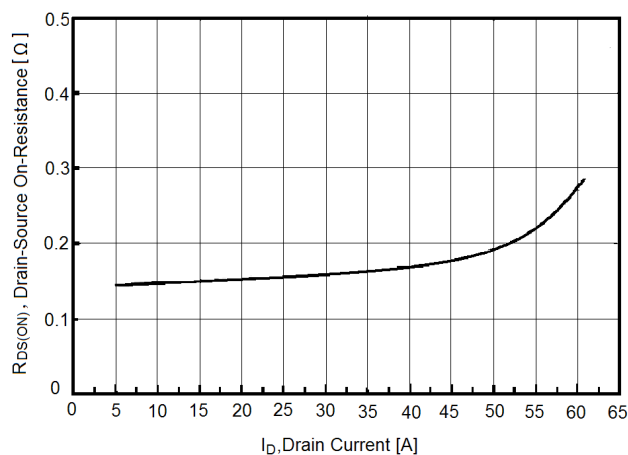


Figure7. $R_{DS(ON)}$ vs Junction Temperature

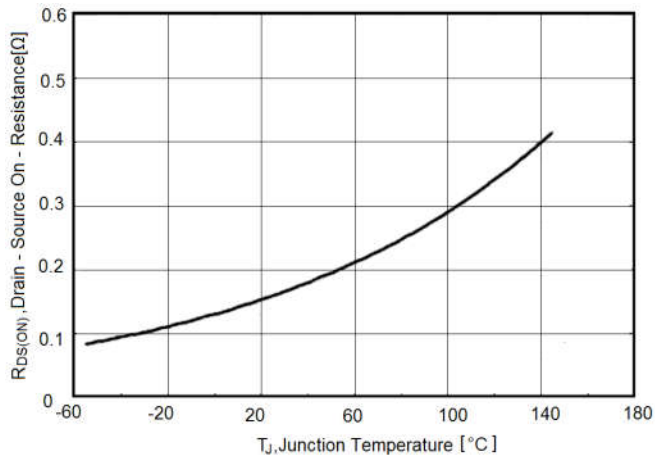


Figure8. BV_{DSS} vs Junction Temperature

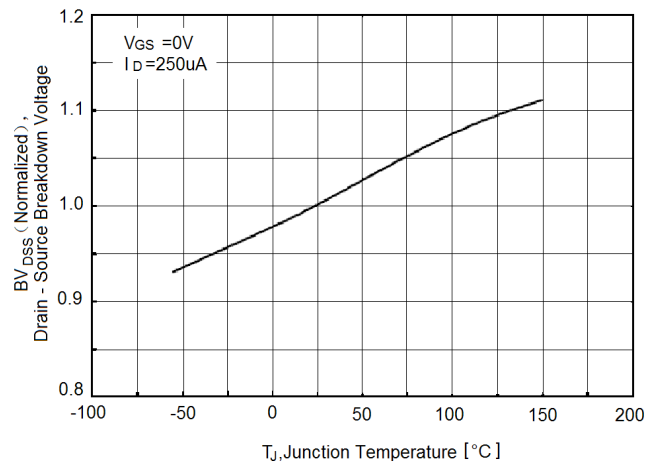


Figure9. Maximum I_D vs Junction Temperature

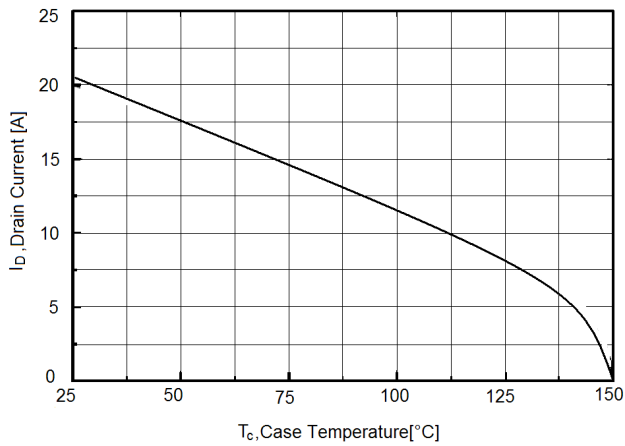


Figure10. Gate charge waveforms

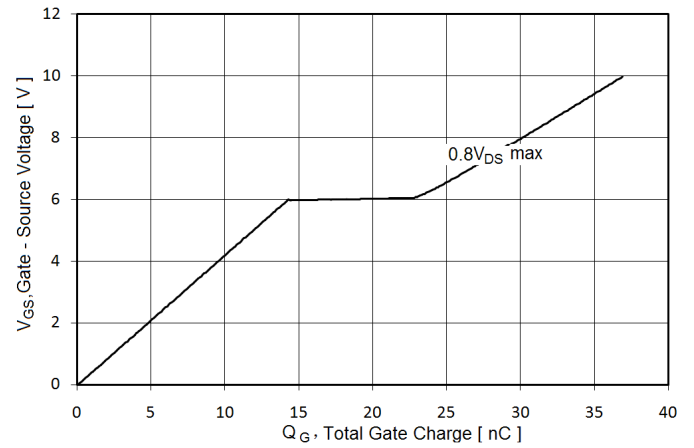
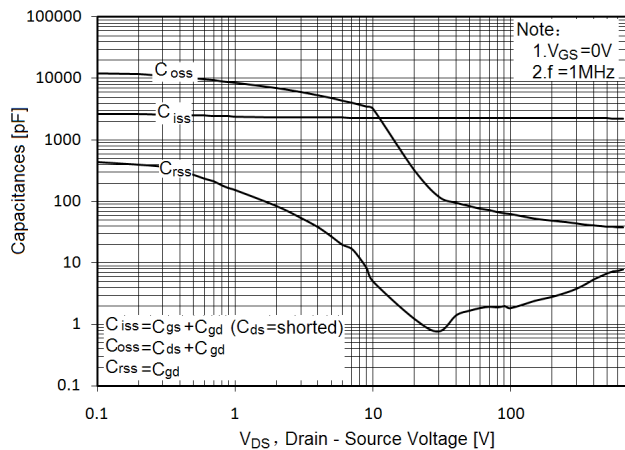
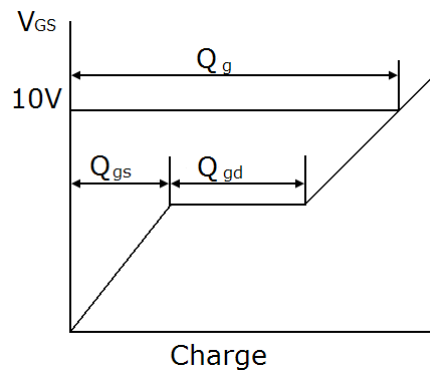
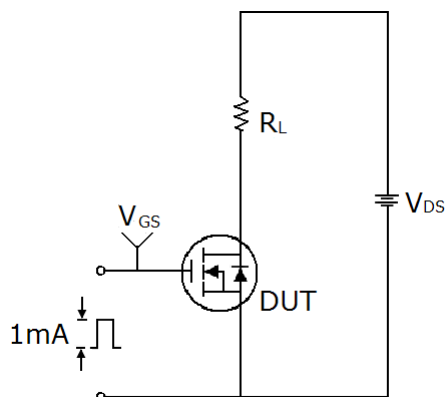


Figure11. Capacitance

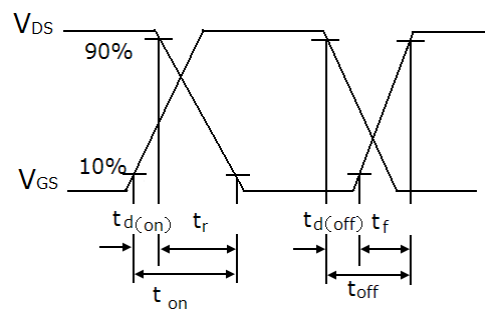
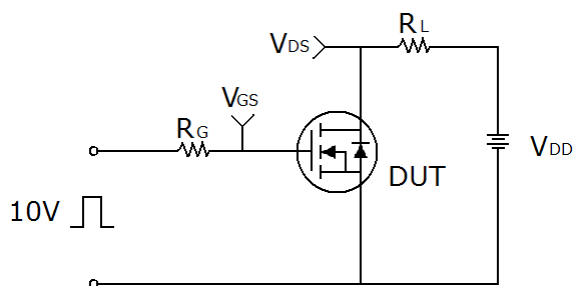


Test circuit

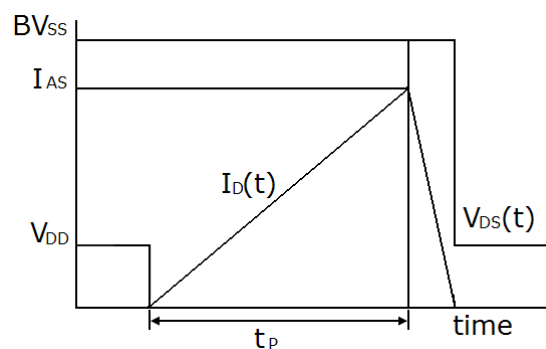
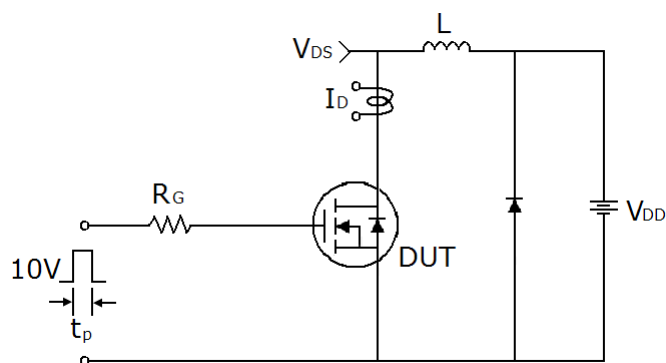
1) Gate charge test circuit & Waveform



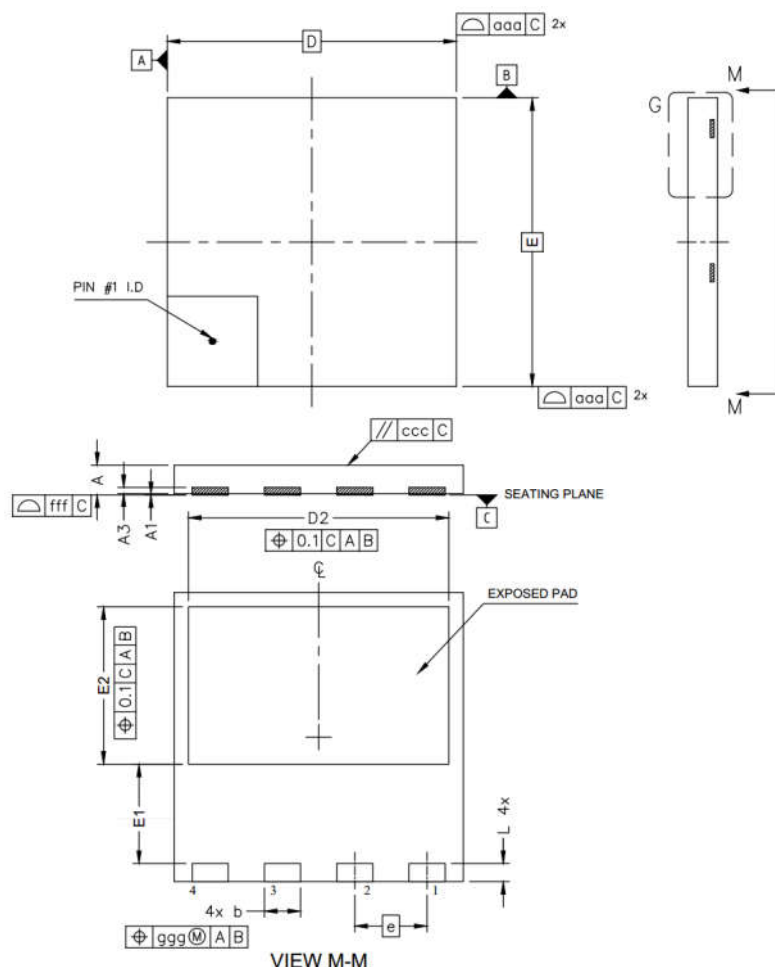
2) Switch Time Test Circuit:



3) Unclamped Inductive Switching Test Circuit & Waveforms



DFN 8×8 Package Information



DIM	MIN	NOM	MAX	NOTES
A	0.75	0.85	0.95	1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994. 2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES. 3.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.90mm AND 1.10mm FROM TERMINAL TIP. 4.0 DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
A1	0.00		0.05	
A3	0.10	0.20	0.30	
b	0.90	1.00	1.10	
D	7.90	8.00	8.10	
E	7.90	8.00	8.10	
D2	7.10	7.20	7.30	5.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL. 6.0 RADIUS ON TERMINAL IS OPTIONAL.
E1	2.65	2.75	2.85	
E2	4.25	4.35	4.45	
e		2.00 BSC		
L	0.40	0.50	0.60	
aaa		0.10		
ggg		0.05		
ccc		0.05		
fff		0.05		

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